Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.041”**



**.006”**

**.004”**

**.004”**

**.041”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004 X .004”**

**Backside Potential: COLLECTOR**

**Mask Ref: DID**

**APPROVED BY: DK DIE SIZE .041” X .041” DATE: 11/16/21**

**MFG: ALLEGRO / SPRAGUE THICKNESS .012” P/N: MPSA42**

**DG 10.1.2**

#### Rev B, 7/1